NON-VOLATILE MEMORY CELL SENSING CIRCUIT, PARTICULARLY FOR LOW POWER SUPPLY VOLTAGES AND HIGH CAPACITIVE LOAD VALUES

Field of the Invention

[0001] The present invention relates to non-volatile memory cell sensing circuits, particularly for low power supply voltages and high capacitive loads. The present invention also relates particularly, but not exclusively, to a memory cell sensing circuit for FLASH-type non-volatile memory devices, and the following description is made with reference to this field of application for convenience of illustration only.

Background of the Invention

[0002] The development of improved processes for manufacturing non-volatile memory cell devices in the CMOS technology field requires the use of lower and lower supply voltages, in some cases close to 1V. In particular, very low supply voltage values are necessary for the use of thinner and thinner oxides. Also, the improved processes should limit as much as possible power consumption in the so-called "design low power" field.

[0003] Nevertheless, there are some requirements that remained basically unchanged despite the evolution in technology which is in contrast with these requirements. On one hand, there is a need to bias

memory cells with drain voltages that are almost constant when technology varies (equal to 1V) in order to keep the current passing through the memory cells in the reading step high. On the other hand, there is a need for low access times even with high capacitive loads due to the large memory cuts required. These two factors make it difficult to manufacture a sensing circuit that is capable of performing a correct bias and I/V conversion for a memory cell in a limited voltage range (Vx).

[0004] A known sensing circuit, with traditional memory cell bias, is schematically shown in Figure 1 and is globally indicated by reference numeral 1. In particular, the sensing circuit 1 is connected to a non-volatile memory cell, illustrated by an equivalent current Ic generator 2 connected to a first voltage reference, such as ground GND.

[0005] Moreover, the sensing circuit 1 is connected to a second voltage reference, such as the supply Vdd, by way of a load 3. The following relation applies to the sensing circuit 1:

$$Vx = Vdd - VBL \qquad (1)$$

where Vdd indicates the circuit supply value and VBL indicates the drain terminal bias voltage of the memory cell corresponding to a voltage value in the contact point between the cell 2 and the sensing circuit 1.

[0006] In known memory devices, particularly in flash memories, the voltage value Vx provided by the above-mentioned relation (1) can be equal, and by way of example, even to only 200mV. The sensing circuit 1 is difficult to manufacture for a correct bias of the

load 3.

[0007] Moreover, to compensate for the reduced drive-capability due to the low supply voltage, it is often necessary to use particular transistors, such as natural transistors. However, these transistors have a higher cost linked to the number of process masks used for their manufacture.

Summary of the Invention

[0008] In view of the foregoing background, an object of the present invention is to provide a sensing circuit for non-volatile memory cells that operates at low supply voltages and for high capacitive loads, and has structural and functional characteristics for overcoming the limits and drawbacks still effecting prior art circuits.

[0009] This and other objects, advantages and features in accordance with the present invention are provided by a sensing circuit comprising a cascode-configured bias circuit and a high efficiency I/V converter. The sensing circuit may operate at supply voltages very close, but not exclusively, to the values which are typical of the bias voltages of the cells manufactured with improved processes.

[00010] On the basis of this solution idea the technical problem is solved by a sensing circuit as previously described and defined in the characterising part of claim 1.

Brief Description of the Drawings

[00011] The features and advantages of the sensing circuit according to the present invention will be apparent from the following description of an

embodiment thereof given by way of a non-limiting example with reference to the attached drawings. In the drawings:

[00012] Figure 1 schematically shows a sensing circuit according to the prior art;

[00013] Figure 2 schematically shows a sensing circuit according to the present invention;

[00014] Figures 3A and 3B schematically show the time trend of voltage values in inner nodes of the sensing circuit of Figure 2; and

[00015] Figure 4 schematically shows an alternative embodiment of the sensing circuit according to the present invention applied to general multilevel memories.

Detailed Description of the Preferred Embodiments

[00016] With reference to the drawings, and particularly to Figure 2, a sensing circuit according to the present invention is globally and schematically indicated by reference numeral 10. The sensing circuit 10 is inserted between a first voltage reference, such as a supply voltage Vdd, and a second voltage reference, such as ground GND. The sensing circuit 10 is connected to an inner circuit node or bitline XBL and to a memory cell 11. The memory cell is represented by a current generator Icell.

[00017] The sensing circuit 10 comprises a bias current Ip generator 12 inserted between the supply voltage reference Vdd and the bitline XBL. The bitline XBL is connected to a matching node Xmat by a cascode-configured bias circuit 13.

[00018] The cascode-configured bias circuit 13 receives as input a voltage reference Vref. The

cascode-configured bias circuit 13 comprises a transistor M1, of the P-channel MOS type, inserted between the bitline XBL and the matching node Xmat. The transistor M1 has a gate terminal connected to an output terminal of an operational amplifier 14. The operational amplifier 14 has a first input terminal for receiving the reference voltage Vref, and a second input terminal connected to the bitline XBL.

[00019] A reference current Iref generator 15 is inserted between the supply voltage reference Vdd and a comparison node Xrif. The matching node Xmat and the comparison node Xrif are connected to ground GND by a current/voltage conversion (I/V) stage 16. The I/V conversion stage 16 comprises a first N-channel MOS transistor M2, which is diode-configured and is inserted between the matching node Xmat and ground GND, as well as a second N-channel MOS transistor M3, inserted between the comparison node Xrif and ground GND and having its gate terminal connected to the gate terminal of the first transistor M2.

[00020] The sensing circuit 10 also comprises a detecting circuit, such as a comparator 17, having the input terminals connected to the matching node Xmat and to the comparison node Xrif. An output terminal OUT of the comparator 17 corresponds to an output terminal of the sensing circuit 10.

[00021] On the basis of the schematic shown in Figure 2, operation of the sensing circuit 10 according to the invention will now be described. The generator 12 supplies the current Ip for biasing the memory cell 11 connected to the bitline XBL during the reading phase, and also for biasing the conversion stage 16 through the transistor M1.

[00022] The difference between the bias current Ip of the generator 12 and the current Icell of the memory cell 11 with respect to a value of the reference current Iref of the generator 15 causes, due to the conversion stage 16 gain, a dynamic change in a value of the voltage Vrif on the comparison node Xrif.

[00023] In particular, the voltage Vrif is compared by the comparator 17 with a voltage Vmat on the matching node Xmat. This depends on a value of the voltage of the memory cell 11 being read that is connected to the bitline XBL.

[00024] In the meantime, the cascode-configured bias circuit 13 performs a fixed bias of the bitline XBL even when the impedance of the memory cell 11 varies. This variation is due to the unknown state of the memory cell 11 being read (a virgin or programmed cell). Therefore, the I/V conversion stage 16 does not disturb the memory cell itself.

[00025] Figure 3A shows the trend of the output feature of the sensing circuit 10 according to the invention, i.e., the trend of the voltage Vrif on the comparison node Xrif with respect to the current Icell flowing in the memory cell 11 by using a supply voltage equal to 1.1V and a bias voltage of the bitline XBL equal to 800mV, as obtained from simulations.

[00026] Similarly, Figure 3B shows the time trend of the voltage values Vmat and Vrif on the matching node Xmat and on the comparison node Xrif, respectively, when the reference current Irif supplied by the generator 15 varies, and of the dynamic feature of the comparator 17 for programmed or virgin memory cells (output indicated in Figure 3B with DATA1[0]).

[00027] On the basis of the results of these

simulations (as shown in Figure 3A), the gain of the sensing circuit is high, particularly when the voltages to be compared are close to each other. This is based upon the sensing circuit comprising the generator 12, the cascode-configured bias circuit 13, the generator 15 and the I/V conversion stage 16 (except for the comparator 17).

[00028] The bias voltage VBL of the bitline XBL is not lost in the bias dynamics of the sensing circuit 10, as in prior art circuits. In fact, the bias voltage VBL of the bitline XBL is advantageously exploited as dynamics for the conversion stage 16 and for the cascode-configured bias circuit 13.

[00029] The use of the cascode-configured bias circuit 13 inserted between the bias part of the bitline XBL (generator 12) and the conversion part (stage 16) makes the sensing circuit 10 according to the invention free with respect to the so-called drain disturb phenomenon, and makes reading operations performed on the cell 11 more reliable.

[00030] It is also possible to extend the operating principle of the sensing circuit 10 according to the invention to a multilevel application, as schematically shown in Figure 4. Figure 4 shows a sensing circuit 100 used in a two-bit per cell application for convenience of illustration. The principle according to the invention may be further extended to n bits per cell.

[00031] The sensing circuit 100 comprises a plurality of branches with a plurality of reference currents Irif1, Irif2, Irif3 connected to a plurality of inputs Xrif1, Xrif2, Xrif3 of an output comparator (not shown). The output comparator also has a further input terminal connected to the matching node Xmat, and a

plurality of output terminals Saout0, Saout1, Saout2.

[00032] In conclusion, the sensing circuit according to the invention allows the difficulties of known circuits to be overcome, by not requiring particular components and completely exploiting the supply voltage Vdd provided. In fact, the sensing circuit according to the invention does not limit the use of the circuitry thereof due to the fixed bias level of the bitline XBL. The sensing circuit allows a correct bias of the memory cell to be performed, and the reading voltage to be set, which is, as it is well known, a critical aspect to avoid the reading drain disturb phenomena.

[00033] The voltage level required to bias the memory device bitlines does not directly effect the definition of the residual voltage used for the I/V conversion and for the stable definition of the bitline level, but is exploited in parallel to this. The choice of drawing the cell current in parallel instead of serially, as in circuits according to the prior art, defines a fixed value that cannot be used for the sensing circuit. In parallel it takes advantage of exploiting all the bitline bias levels, now close to the supply value, to perform both the I/V conversion and the cascode operation required to set the bitline voltage and the capacitive decoupling.